Docket No.: FI9-97-205US2
(20136-00318-US)
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Cyprian E. Uzoh, et al.

Application No.: 09/611,955 | Confirmation No.: 6678

Filed: July 6, 2000 | Art Unit: 2818

For: METHOD TO SELECTIVELY FILL RECESSES WITH CONDUCTIVE METAL | Examiner: H. Vu

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an appeal from the Primary Examiner's Final Rejection of claims 25-32.

This brief is transmitted in triplicate.

This brief contains items under the following headings as required by 37 C.F.R. § 1.192 and M.P.E.P. § 1206:

I. **Real Party In Interest**

The real party in interest is International Business Machines Corporation.

II. **Related Appeals and Interferences**

There are no related appeals or interferences known to appellant, appellant's legal representative or assignees which will directly affect or be directly affected by or having a bearing on the Board's decision in this appeal.

III. **Status of Claims**

Claims 1-32 are pending in the application.

Claims 25-32 are on appeal.

Claims 1-24 have been cancelled.

IV. **Status of Amendments**

No amendment to the claims was filed after the Final Rejection.

V. **Summary of Invention**

The present invention relates to a semiconductor structure. The semiconductor structure of the present invention comprises a semiconductor substrate (see page 6, line 13 and page 22, original claim 25 lines 1 and 2), a recess located in at least one major surface of the semiconductor substrate (see page 1, lines 14-16; page 22, original claim 25, lines 2 and 3; and original abstract of disclosure);

an electrical insulating layer located over the at least one major surface and in said recess (page 7, lines 20-23);

a conductive barrier located over the insulating layer in the recess and over the at least one major surface (page 8, lines 1 and 2);

a plating seed layer over the conductive barrier within the recess only (page 6, lines 17-19; page 8, lines 18-19; original claim 25, lines 5-7); and

a conductive metal in the recess only (page 6, lines 19-20; page 10, lines 4-5; page 23, original claim 25, lines 7-8).

VI. Issues on Appeal

A. Do claims 25 and 31-32 and the specification contain new matter in the recitation "recess located in at least are major surface of said semiconductor substrate"?

B. Are claims 25-32 enabled by the specification and therefore in compliance with 35 U.S.C. § 112, first paragraph, in the recitations "a conductive barrier located over said insulation layer in said recess and over said at least one major surface" and "a conductive metal in said recess only"?

C. Are claims 25, 28-29 and 31-32 anticipated by U.S. Pat. No. 5,821,168 to Jain and therefore unpatentable under 35 U.S.C. § 102(e)?

VII. **Grouping of Claims**

For each rejection, those claims that are involved stand or fall together.

VIII. **Appellant's Arguments**

A. Claims 25 and 31-32 and the specification do not contain any new matter.

Claims 25 and 31-32 and the specification were objected as containing new matter in the recitation "recesses located in at least one major surface of said semiconductor substrate".

The objection to the specification as containing new matter and the objection to claims 25 and 31-32 are not deemed tenable. The specification as originally filed explicitly discloses that recesses are formed in at least one major surface of the semiconductor substrate. For instance see page 1, lines 14-16 of the original disclosure that state:

> "This is achieved by selectively plating recesses in a semiconductor substrate with conductive metal such as cooper or gold."

Also, see original claim 25 as filed which states "recesses located in at least one major surface of said semiconductor substrate." In addition, see the original Abstract of the Disclosure that that states:

> "Recesses in a semiconductor structure are selectively plated..."

Accordingly, the above recitation is not new matter and claims 25, 31 and 32 properly recite "in".

B. Claims 25-32 are in compliance with the enablement requirements of 35 U.S.C. § 112, first paragraph.

Claims 25-32 were rejected under 35 U.S.C. § 112, first paragraph based upon non-enablement in the recitations "a conductive barrier located over said insulation layer in said recess and over said at least one major surface" and a conductive metal in said recesses only". This rejection is not deemed enable.

The specification expressly discloses providing a conductive barrier located over the insulation layer. For example, page 8, lines 1 and 2 state:

> "Next, a conductive barrier 4 is provided over the insulating layer." Also see Figures. 3 and 4.

The specification also expressly discloses "a conductive metal in said recesses only." Along these lines, see page 6, lines 19-22, which states:

> "An electroplated conductive metal is located in the recesses only... and not on other portions of the substrate."

Also see page 10, lines 9 and 10, which states:

> "The conductive metal does not plate on the barrier layer but instead preferably plates on the seed layer." The seed layer

> remains in the recesses only (see page 6, lines 18-19).

On the other hand, the Examiner relies upon the statement in the specification "conductive barrier located over said at least one major surface." However, this reference to the "conductive barrier located over said at least one major surface" refers to structure as shown in Figure 7 which illustrates barrier layer 4 located over at least one major surface as well as an intermediate structure that would exist between Figures 3 and 4, prior to removal of the barrier layer down to the insulating layer. For instance, see page 12, lines 11-27 of the original disclosure that states:

> "The conductive material 8 can then be chemically-mechanically polished to remove small amounts of metal above the surface of the recesses. Typical polishing slurries contain colloidal silica. Next, the barrier layer 5 and plated metal is removed down to the insulating layer 3 (see Fig. 4)." (emphasis mine)

C. Claims 25, 28-29 and 31-32 are not anticipated by Jain.

Claims 25, 28-29 and 31-32 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 5,821,168 to Jain.

Jain does not anticipate the above claims, since, among other things, the recesses 72 in insulating layer 52 of Jain do not exist in a semiconductor substrate as recited in the claims. The recesses exist only on the substrate.

Accordingly, Jain fails to anticipate the present invention. In particular, anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. *See Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir. 1985), *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 1 USPQ2d 1081 (Fed. Cir. 1986), and *Akzo N.V. v. U.S. International Trade Commissioner*, 1 USPQ2d 1241 (Fed. Cir. 1986).

There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. 102. *See Scripps Clinic and Research Foundation v. Genetech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

Conclusion

In view of the above, it is abundantly clear that the Primary Examiner erred in finally rejecting claims 25-32. It is therefore respectfully requested that the Board reverse the Examiner and allow claims 25-32.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to Deposit Account No. 09-0458, under Order No. 20136-00318-US from which the undersigned is authorized to draw.

Dated: 11-25-03

Respectfully submitted,

By _____

Burton A. Amernick, Reg. No. 24,852
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 09/611,955

25. (Previously presented) A semiconductor structure, comprising: a semiconductor substrate; a recess located in at least one major surface of said semiconductor substrate; an electrical insulating layer located over said at least one major surface and in said recess; a conductive barrier located over said insulating layer in said recess and over said at least one major surface; a plating seed layer located over said conductive barrier within said recess only; and a conductive metal in said recess only.

26. (Original) The semiconductor structure of claim 25 wherein said barrier comprises a layer of tantalum nitride adjacent said insulating layer and a layer of tantalum above said tantalum nitride layer.

27. (Original) The semiconductor structure of claim 26 wherein said tantalum nitride layer is about 15 to about 500 Å thick and said tantalum layer is about 500 to about 5000 Å thick.

28. (Original) The semiconductor structure of claim 25 wherein said seed layer is copper.

29. (Original) The semiconductor structure of claim 28 wherein said copper is sputtered copper.

30. (Previously presented) The semiconductor structure of claim 28 wherein said copper is about 100 to about 2000 Å thick.

31. (Previously presented) The semiconductor structure of claim 25 wherein said conductive metal is copper.

32. (Previously presented) The semiconductor structure of claim 31 wherein said conductive metal is about 4000 Å to about 30,000 Å thick.